ABSTRACT

The disclosure includes a description of a content addressable memory (CAM) that includes at least one tag input and at least one random access memory. The CAM also includes circuitry to perform multiple read operations of the at least one random access memory with multiple, different ones of the read operations specifying an address based on different subsets of tag bits. The circuitry includes digital logic circuitry coupled to the at least one random access memory to determine whether a lookup tag matches a subset of the different subsets of tag bits.